LISTING OF CLAIMS

1. (Currently Amended) A method, comprising:

monitoring a state of a[[n]] **multi-threaded** application running in a system~~, including monitoring one or more~~ **and a** buffer[[s]] associated with the **multi-threaded** application**, wherein each thread includes one or more activities to be executed by the system**;

~~monitoring a machine state of the system, including~~ determining ~~the~~ availability of ~~configurable hardware components in the system, wherein the configurable hardware components include at least~~ a processor ~~that~~ **to** perform[[s]] simultaneous multi-threading and [[a]] **the** buffer;

coordinating dispatch of ~~a plurality of~~ threads **of the multi-threaded application** ~~in the system at least in part~~ to increase execution overlap of ~~the threads, wherein at least one of the threads is associated with the application~~ **activities executing in the system based, at least in part, on the availability of the buffer**;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based**,** at least **in part,** on the ~~state of the application and the state of~~ **availability of the buffer and the coordination of the dispatch of** the threads; and

dynamically adjusting the buffer size based**,** at least **in part,** on the ~~state of the application and the state of the threads in the system~~ **adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads**.

2. (Currently Amended) The method of claim 1, wherein ~~a thread includes one or more activities, and wherein said~~ coordinating dispatch of the threads ~~in the system~~ **of the multi-**

threaded application includes assessing execution readiness of the one or more activities **of each thread**.

3. (Currently Amended) The method of claim 2, wherein ~~said~~ coordinating dispatch of the threads ~~in the system~~ **of the multi-threaded application** includes delaying a ready-to-be-dispatched activity from being dispatched.

4. (Currently Amended) The method of claim 3, wherein a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities ~~can be~~ **are** dispatched together, and wherein the first and second activities are from one or more applications.

5-6. (Cancelled)

7. (Currently Amended) The method of claim [[6]]**1**, **further comprising**

~~wherein the~~ **determining the availability of** configurable hardware components ~~further include,~~ **including** ~~hardware buffers, memory, cache,~~ **an** arithmetic logic unit (ALU), and registers in the system**, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components**.

8-9. (Cancelled)

10. (Previously Presented) The method of claim 7, wherein adjusting the voltage applied to the processor includes powering on or powering off at least a portion of circuitry in the system.

11. (Currently Amended) The method of claim 1, wherein ~~said~~ monitoring the ~~one or more~~ buffer[[s]] associated with the **multi-threaded** application includes monitoring buffer fullness levels of the ~~one or more~~ buffer[[s]].

12. (Currently Amended) The method of claim 11, wherein ~~said~~ monitoring the buffer fullness levels includes~~, for each buffer associated with the application,~~ comparing [[a]] **the** buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

13. (Currently Amended) The method of claim 12, wherein ~~said~~ comparing ~~is to determine~~ **the buffer level includes determining** buffer overflow and buffer underflow conditions **based, at least in part, on the high level mark and the low level mark**.

14. (Currently Amended) A computer readable storage medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of a[[n]] **multi-threaded** application running in a system~~, including monitoring one or more~~ **and a** buffer[[s]] associated with the **multi-threaded** application**, wherein each thread includes one or more activities to be executed by the system**;

~~monitoring a machine state of the system, including~~ determining ~~the~~ availability of ~~configurable hardware components in the system, wherein the configurable hardware components include at least~~ a processor ~~that~~ **to** perform[[s]] simultaneous multi-threading and [[a]] **the** buffer;

coordinating dispatch of ~~a plurality of~~ threads **of the multi-threaded application** ~~in the system at least in part~~ to increase execution overlap of ~~the threads, wherein at least one of the threads is associated with the application~~ **activities executing in the system based, at least in part, on the availability of the buffer**;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based**,** at least **in part,** on the ~~state of the application and the state of~~ **availability of the buffer and the coordination of the dispatch of** the threads; and

dynamically adjusting the buffer size based**,** at least **in part,** on the ~~state of the application and the state of the threads in the system~~ **adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads**.

15. (Currently Amended) The computer readable storage medium of claim 14, wherein ~~said~~ coordinating dispatch of the threads ~~in the system~~ **of the multi-threaded application** includes delaying a ready-to-be-dispatched activity from being dispatched.

16-18. (Cancelled)

19. (Currently Amended) The computer readable storage medium of claim 14,

wherein monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer, and wherein ~~said~~ monitoring the buffer fullness levels includes~~, for each buffer associated with the application,~~ comparing [[a]] **the** buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

20-38. (Cancelled)

39. (Currently Amended) A system, comprising:

a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor ~~comprising~~ **to include** a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, said sequence of instructions to cause said execution unit to:

monitor a state of a[[n]] **multi-threaded** application running in a system~~,~~ ~~including monitoring~~ buffer ~~fullness levels of one or more buffers~~ associated with the **multi-threaded** application**, wherein each thread includes one or more activities to be executed by the system**;

~~monitor a machine state of the system, including determining~~ **determine** ~~the~~ availability of ~~configurable hardware components in the system, wherein the configurable hardware components include at least~~ a processor ~~that~~ **to** perform[[s]] simultaneous multi-threading and [[a]] **the** buffer;

coordinate dispatch of ~~a plurality of~~ threads **of the multi-threaded application** ~~in the system at least in part~~ to increase execution overlap of ~~the threads, wherein at least one of the threads is associated with the application~~ **activities executing in the system based, at least in part, on the availability of the buffer**;

dynamically adjust one or more of the frequency or the voltage applied to the processor based, at least **in part,** on the ~~state of the application and the state of~~ **availability of the buffer and the coordination of the dispatch of** the threads; and

dynamically adjust the buffer size based, at least **in part,** on the ~~state of the application and the state of the threads in the system~~ **adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads**.

40. (Currently Amended) The system of claim 39, wherein said coordinating dispatch of the threads ~~in the system~~ **of the multi-threaded application** includes delaying a ready-to-be-dispatched activity from being dispatched.

41-43. (Cancelled)

44. (Currently Amended) A system, comprising:

a multi-threading processor; and

a resource manager coupled to the multi-threading processor, the resource manager is to monitor states of a[[n]] **multi-threaded** application running in the system, the states of the application including buffer fullness levels of one or more buffers used by the application, the

resource manager is to further monitor states of ~~a plurality of~~ **the** threads **of the application** in the system for execution readiness, wherein the resource manager is to

increase or decrease resources available in the system depending on the state of the application and/or the states of the threads in the system**, and**.

change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based, at least in part, on the buffer fullness levels.

45. (Cancelled).

46. (Currently Amended) The system of claim [[44]]**45**, wherein the resource manager is to **further** change the execution readiness of a thread from a ready state to a queued state to increase subsequent system idle time when there is no thread execution.

47. (Original) The system of claim 46, wherein the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers.

48. (Currently Amended) An apparatus, comprising:

a processor capable of simultaneous multi-threading , the processor having logic to monitor states of a[[n]] **multi-threaded** application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application;

logic to monitor states of ~~a plurality of~~ **the** threads **of the application** in the system for execution readiness;

logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system **and to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage**; and

a memory to store the logic.

49. (Original) The apparatus of claim 48, further comprising:

logic to change the execution readiness of a thread from a ready state to a queued state when it is determined that there is no other thread running or ready to be dispatched.

50. (Cancelled).